PERFORMANCE EVALUATION FOR JAPAN ISDB-T 1SEG SDR PROCESSING

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ABSTRACT

In order to develop the multi wireless communication services by hardware, the cost and time have been increased and circuit size becomes large. Therefore Software defined radio (SDR) is a quite attractive field of research since it can reduce time consuming prototype development time from research themes. SDR can replace hardware problem by software problem since it define wireless communication system including the radio processing parameter by software. This paper presents the architecture of the back-end of "1seg" receiver with the C-language program is configurable. "1seg" receiver developed by SDR turned out to be feasible technology according to the evaluation of CPU execution time.

Index Terms— Software defined radio, SDR, OFDM, ISDB-T, 1seg, Oneseg, One-seg

1. INTRODUCTION

In recent years, various radio communication systems such as a cellular phone, wireless LAN, TV boroadcasting are investigated and developed separately by making use of advance of semiconductor technologies. Since each radio system is implemented with separate hardware components, system size becomes large and development cost and time have been increased in case to support multi wireless communication services. Therefore the Software Defined Radio (SDR) system attracts attention. Since most public software player is Personal Computer (PC) and size of PC is expected to be much small size, it is expected that PC will be used as a SDR terminal with minimum addition of hardware components. Currently, high bandwidth communication system adopt Orthogonal Frequency Division Multiplex (OFDM) modulation. Then, this paper shows SDR implementation results of Japan Digital TV 1seg receiver system by PC with software programming.

The contents of this paper is organized as follows. Section 2 is about architecture of 1seg receiver developed by SDR. Section 3 is measurement result. The conclusion is given in Section 4.

2. ARCHITECTURE

2.1. ISDB-T 1seg SDR

Software Defined Radio (SDR) is the technique of getting code as close to the antenna as possible for radio communication system. SDR performs all process of radio communication after ADC (Analog to Digital Converter) by software. It turns radio hardware problems into software problems. Fig.1 shows schematic image of SDR. SDR technology brings the flexibility, cost efficiency with wide variety of benefits realized by service providers and product developers through to end users. ISDB-T (Integrated Services Digital Broadcasting - Terrestrial) is advanced international standard on digital terrestrial television broadcasting format originally developed in Japan. It can broadcast simultaneously HDTV and "1seg" programs. One channel for ISDB-T is divided into 13 segments in frequency scale, 12 segments are utilized for HDTV and The single one of center of segments is for "1seg". "1seg" is the name of a broadcasting service for handheld receivers such as cellular phones, which means small display size and fewer frame per seconds. Fig.2 describes channel segments allocation of ISDB-T. Since sub-carrier spacing of ISDB-T is $\sim$992Hz, 433 sub-carriers are used in 1seg service.

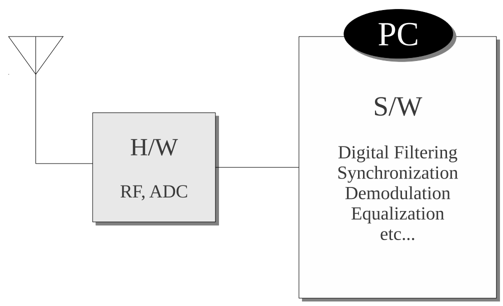


Fig. 1. SDR

2.2. Software partitioning

It is assumed that after the analog front-end processing, 1seg digital TV signal is digitized and available in PC. Fig.3 shows the simple block diagram of the 1seg receiver SDR system.

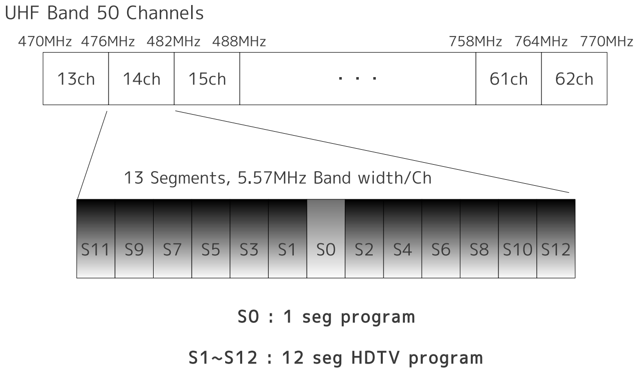


Fig. 2. ISDB-T

The input signal is down-converted by FLO/RSMP (Frequency local Oscillator/Re-SaMPle) to generate baseband signal such as complex (a+bj). In this prototype, input signals sampling frequency F_S=4.0Msps is assumed by taking real available 1seg tuner products into account. Because of ISDB-T "1seg" specification, sampling frequency at FFT (Fast Fourier Transform) F_S=1.0158Msps is necessary. In the first function block FLO/RSMP, baseband signal generation and sampling frequency conversion (re-sample) from 4.0MHz to 1.0158MHz is performed. The second function block DEROT does de-rotates the re-sample outputs to compensate radio frequency error. FLO, RSMP and DEROT are called digital front-end processing. In our approach, SSYNC, FFT and EQ is called digital demodulation. The detail functions of the components are described following sections (from 2.3 to 2.5).

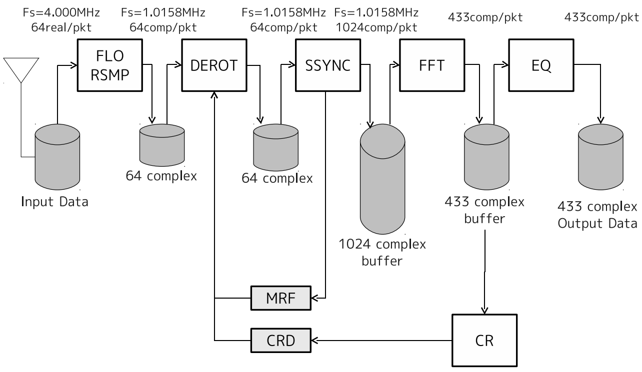


Fig. 3. Simplified block diagram of 1seg SDR processing

2.3. SSYNC

The main task of SSYNC (Symbol SYNChronization) is to detect correct FFT window position. Since 1seg uses ccyclic prefix OFDM signal, the prefix portion namely Guard Interval (GI) can be uses to detect the window position. Assume N_{PD} is OFDM signal length (1024 points), the correlation can be computed as equation (1) proposed by [1]. Fig.4 describes the image of correlation by equation (1). Simultaneously, SSYNC detects radio frequency error to feedback the error to DEROT. By making a feedback loop between DEROT and SSYNC, radio frequency error compensation and tracking mechanism are implemented. SSYNC receive the input data into buffer,then outputs the data which is adjusted to FFT window size after success of symbol synchronization.

$$\begin{aligned}\Lambda_s(k_\epsilon) &= \sum_{i=0}^{N_P-1}\left\{|r(k_\epsilon)|^2+|r(k_\epsilon+N_{PD})|^2\right\} \\ &\quad -2\left|\sum_{i=0}^{N_P} r(k_\epsilon+i+N_{PD})\cdot r^*(k_\epsilon+i)\right| \quad (1)\end{aligned}$$

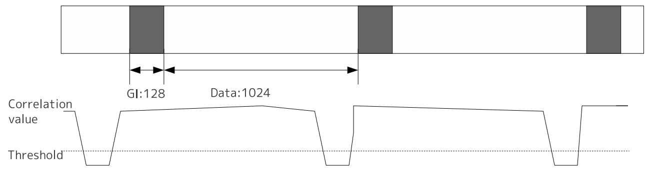


Fig. 4. Correlation image

2.4. FFT

FFT (Fast Fourier Transform) converts time-domain signal into frequency domain. This is the demodulation process on OFDM, because orthogonal sub-carriers are used to carry symbol data. Equation (2) represents the FFT calculation. Equation (2) can change into equation (4) when W_n is defined by eqation (3).

$$X(n) = \sum_{n=0}^{N-1} x(n)\cdot e^{-j(\frac{2\pi}{N})nk}(k=0,1,\ldots,N-1) \quad (2)$$

$$W_N = e^{-j(\frac{2\pi}{N})} \quad (3)$$

$$X(k) = \sum_{n=0}^{N-1} x(n)\cdot W_N^{nk}(k=0,1,\ldots,N-1) \quad (4)$$

One OFDM time-domain symbol length is 1008μs. Then 1024 point FFT with F_S=1.0158MHz is required. From FFT output of 1024 complex points, necessary 1seg " sub-carriers of 433 points are transfered to succeeding EQ block. 1024 FFT is expressed in equation 5

$$X(k) = \sum_{n=0}^{1023} x(n)\cdot W_{1024}^{nk} \quad (5)$$

The computation of FFT block is based fixed point processing and Radix-4 multi-stage computation algorithm is used. 1024 FFT in Radix-4 multi-stage computation is expressed in equation (8) when k and n are defined by equation (6)(7)

$$k = k_0 + 4k_1 + 16k_2 + 64k_3 + 256k_4 \quad (6)$$

$$n = n_0 + 4n_1 + 16n_2 + 64n_3 + 256n_4 \quad (7)$$

$$(k_0, k_1, k_2, k_3, k_4 = 0, 1, 2, 3)$$

$$(n_0, n_1, n_2, n_3, n_4 = 0, 1, 2, 3)$$

$$X(k) = \sum_{n_0=0}^{3}\sum_{n_1=0}^{3}\sum_{n_2=0}^{3}\sum_{n_3=0}^{3}\sum_{n_4=0}^{3} x(n)W_{1024}^{nk} \quad (8)$$

2.5. EQ

In EQ (EQualizer), there are two main functions. The one is channels estimation and the other is to remove signal distortion by the channel estimation result. Since the FFT outputs of 433 points includes 36 scattered pilot (SP) points, Channel Transfer Function (CTF) can be computed by the interpolation calculation. By divide the FFT output data by the CTF, signal distortion can be compensated. This process is called as Equalization. In this implementation, 2-dimensional interpolation is used such as time domain linear interpolation and frequency domain interpolation. Originally every 12 subcarriers arranged SP are time-interpolated to generate every 3 sub carriers position. After the freauency domain interporation, all position value (CTF) are available. CTF acquirement appearance is shown as Fig.5.

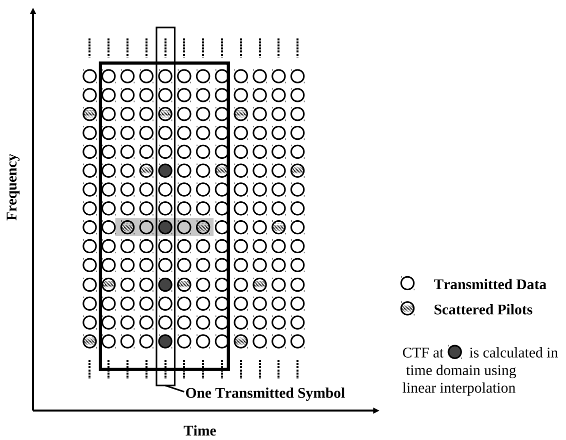


Fig. 5. Equalization

3. MEASUREMENT RESULT

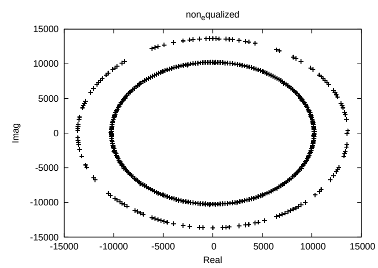
Processing performance of the proposed system is measured by CPU execution time. Table.1 describes specifications of the use PC platform. OFDM parameter of 1seg can be referred to [2].

Table 1. Simulation specifications

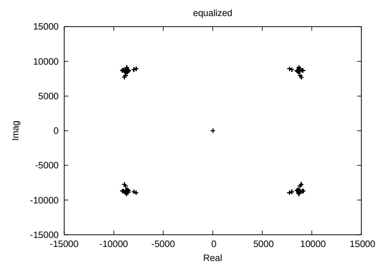
Machine Specification	
OS	Ubuntu 9.10
CPU	Intel Core 2 Duo 3.06 GHz
Memory	4.00 GB
Language	C
Compiler	gcc version 4.4.1
OFDM parameter	
FFT window size	1024
Symbol size	1008 μs
Sub-carrier number	433
Channel	1-wave, No noize

3.1. Symbol Constellations

Fig.6 shows the obtained constellations. Fig.6 (a) shows the outputs of FFT, and Fig.6 (b) shows the outputs of EQ. Used test signal vectors are separately generated by Signal Processing Software which is stored in PC memory. SSYNC block successfully detects FFT window position and pass data to FFT. Since the detected FFT window position is inside GI then, rotation of the signal is observed (see Fig.6 (a)). On the other hand, a quantity of phase shifting has been showned in Fig.6 (b), however, clean QPSK constellation is observed. So it can be said that correct symbol data can be obtained from outputs of EQ.



(a) Non equalized constellation



(b) Equalized constellation

Fig. 6. Comaprrison of non-equalization and equalization

3.2. CPU Execution Time

Fig.7 shows the bar graph of execution time through three functions (SSYNC, FFT, EQ) with 100 symbols in the test data. GCC compiler is utilized in this evaluation. GCC compiler has optimization options "-Ox", and there are some optimization levels (x is the level). The following is the feature of each optimization options which is refered to [3].

- -O option

  With -O, the compiler tries to reduce code size and execution time, without performing any optimizations that take a great deal of compilation time.

- -O2 option

  Optimize even more. GCC performs nearly all supported optimizations that do not involve a space-speed tradeoff. As compared to -O, this option increases both compilation time and the performance of the generated code.

- -O3 option

  Optimize yet more. -O3 turns on all optimizations specified by -O2 and also turns on the -finline-functions, -funswitch-loops, -fpredictive-commoning, -fgcse-after-reload and -ftree-vectorize options.

One OFDM symbol length of 1seg is 1008μs. In order to realize real time demodulation process using PC, at least 100 symbol processing has to finish within 1008μs $\times$ 100 second. Without the optimization option, it do not satisfy the condition. However, it can satisfy this condition when the compiler optimize its C program.

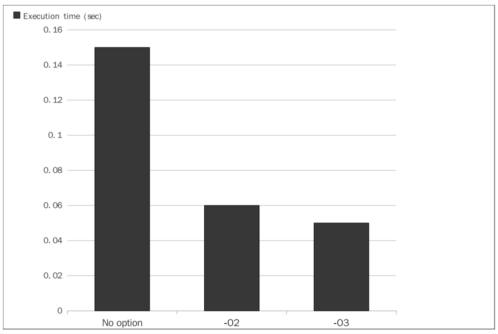


Fig. 7. Execution time by each gcc options

4. CONCLUSION

This paper proposed Japan ISDB-T 1seg receiver architecture in C programing. Simulation results showed that it's able to implement SSYNC, FFT, EQ components in SDR. The testbench marks 0.05 sec to handle 100 OFDM symbols. So it can be said that 1seg receiver which is developed by SDR can be realize.

5. REFERENCES

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[3] Richard M. Stallman and the GCC Developer Community, *Using the GNU Compiler Collection*, GNU Press a division of the Free Software Foundation, for gcc version 4.4.4 edition, 2003.