A 2/4/8 antennas configurable diversity OFDM receiver for mobile HDTV Application

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Abstract

Two array antennas and one carrier diversity combiners are integrated with Japan Terrestrial digital TV (ISDB-T) OFDM receiver using 90nm 7M1P CMOS process. A 2/4/8 antennas diversity receiver can be configured and the low cost 4 antennas diversity reception system can be realized by one LSI. The mobile reception performance is increase by 63% using de-noise filter circuit and SPLINE interpolator. The die area is 49mm^2 and the power consumption is 310mW.

Keywords: mobile reception, OFDM, array antenna, diversity.

Introduction

The TV broadcasting technology is rapidly shifting to digital domain and the services are expanding not only to home TV but also to ubiquitous devices such as cellar phones, PCs, automotive TVs. In order to realize a High Definition TV reception service in a mobile environment, multi-antenna diversity receiver is essential to enhance SN Ratio (SNR) and to mitigate a deep-null multi-path fading. A mobile OFDM receiver is developed which includes two time domain array antenna (AA) combiners and a frequency domain carrier diversity (CD) combiner. The receiver supports the maximum 23.234Mbps stream for a MPEG2 encoded HDTV reception service in 5.7MHz UHF channels at 120km/h speed by 2 antennas CD mode.

Proposed Architecture

Fig. 1 shows the detailed block diagram of the receiver. The UHF wireless signal is down-converted by tuners. Max 4 tuner output signals are fed into the receiver and are converted to digital signals by ADCs. The first AA stage performs the array antenna signal processing [1] and the second CD stage combines each OFDM sub-carrier signal which is the output of

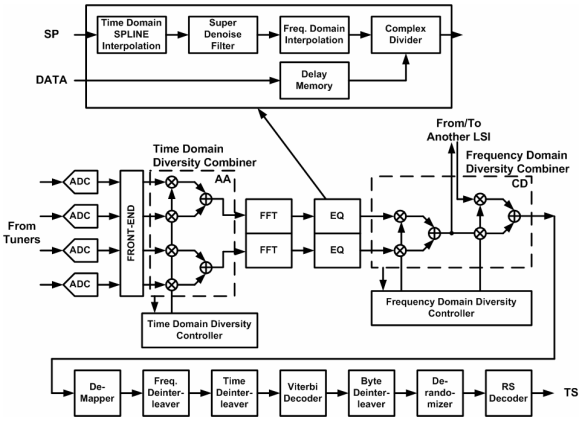

Fig. 1 Detailed Block Diagram of the Receiver

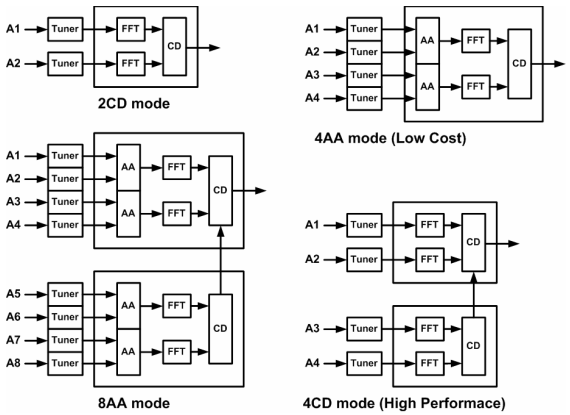

Fig. 2 2/4/8 antennas System Configurations

the Fast Fourier Transforms (FFT) / equalizers (EQ). The two stage diversity combiners halve the number of FFT/EQ circuits from 4 to 2 and sustain similar mobile reception performance comparing with 4 FFT/EQs case. Consequently, 39% logic gates are reduced by the two stage architecture. To achieve a higher mobile performance, the equalizer introduces two new circuit blocks, the SPLINE interpolator and the super de-noise filter.

4 kinds of diversity configurations are possible as shown in fig. 2. Every time doubling the number of antennas, roughly 3dB SNR is improved. For 4 antennas case, there are two possible configurations. The 4AA mode is a one chip solution to achieve the lowest cost and modest performance. The 4CD mode is a two chip solution for higher performance. Since the antenna space on a car is usually on the front or back side glasses, each antenna gain has directional fluctuation by influence of a car body. The 4 antennas system is preferable for compact to medium range cars to cover all angles of arrival signals.

Fig. 3 shows the newly introduced SPLINE interpolator. The sub-carrier signals (see left) of FFT output are divided into two parts, data and scattered pilots (SPs, P in the circle). Those SPs are located every 12 sub-carriers in one OFDM symbol and the position of SP shifts by 3 sub-carriers every OFDM symbol. In the previous work [2], 2-taps linear interpolation is performed by the two SPs in linear interpolation zone. Here, the new SPLINE algorithm 4-taps interpolation is applied. Although the SPLINE uses two more past SPs in SPLINE interpolation zone (total 4 taps), the 3 symbols of the filter latency (see symbol number = -3) is the same as the previous work. Then the higher interpolation accuracy is obtained while avoiding from increasing the delay RAM size in equalizer (see fig. 1). The 4-taps FIR filter is implemented by a poly-phase accumulator.

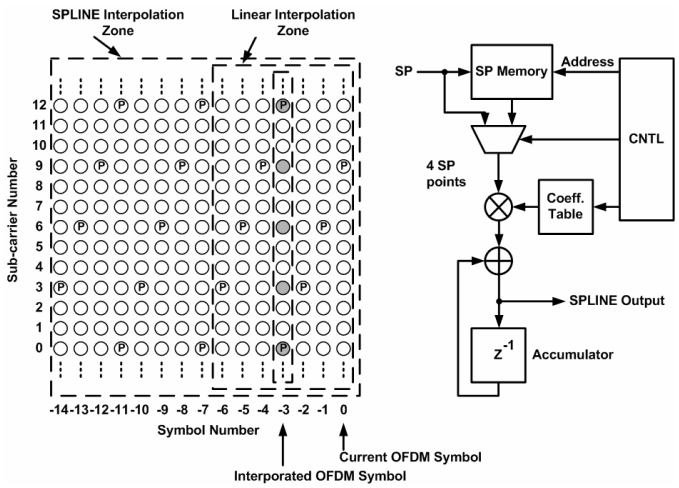

Fig. 3 SPLINE time domain interpolator

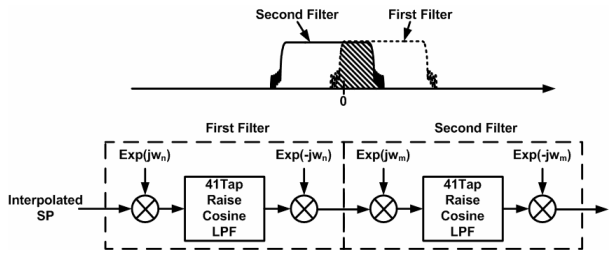

Fig. 4 Variable Bandwidth Super De-noise Filter

To further reduce noise on the interpolated SP signals, variable bandwidth complex band-pass filter is newly introduced. The bandwidth and the frequency position have to be controlled by a delay-profile of the reception signal. To support fine control of the frequency position and a broad range of the filter bandwidth, two stages serially connected circuit is used as shown in fig.4. Both stages are identical 41-taps raised cosine LPFs. Each stage band-pass position can be shifted by the complex rotation circuit, that is, complex multiplier at each input/output. By the combination of the two stages, the complex filter bandwidth and frequency position can be controlled. The upper of fig. 4 shows the example of a 1/4 bandwidth of the LPF. The shaded area is complex band-pass filter bandwidth.

Measurement Results

Thanks to the newly introduced circuits, the maximum Doppler performance is improved from 41Hz to 67Hz at the condition of typical urban 6 paths Rayleigh fading (TU6) model with 2CD mode as shown in fig. 5. The 1.63 times improvement corresponds to the moving speed improvement from 73km/h to

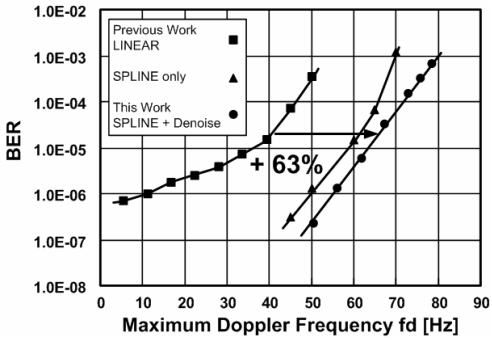

Fig. 5 Mobile Reception performance comparison of 2CD mode

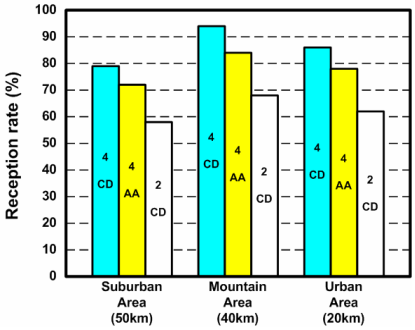

Fig. 6 Field Experiment Result

120km/h at UHF35ch (605.143MHz).

The actual mobile reception performance was measured by field experiment at three severe test courses in Osaka Japan. Fig. 6 shows the reception rate (error free reception duration to the total experiment duration) of those test courses. The experimented UHF channel is 13ch which is broadcasted from the top of Ikoma Mountain between Osaka and Nara prefecture. 64QAM, code rate of 3/4, 12 segments HDTV broadcasting service are used. One chip solution 4AA mode showed very close performance to the two chip solution 4CD mode.

Summary

Fig. 7 shows the die micrograph and summary. Two array antennas and one carrier diversity combiner are integrated with ISDB-T OFDM receiver in 90nm 7M1P CMOS process occupying 49mm^2 and dissipating 310mW. The two stage diversity combiners reduced 39% of logic circuits comparing with a conventional 4 FFT/EQs carrier diversity. The total logic size and the memory size are 18M gates and 18.4M bit, respectively. The package is 12mm square 144pin fine pitch ball grid array.

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References

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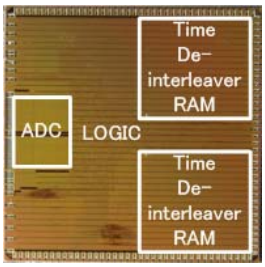

Process Technology	90nm 7M1P CMOS
Logic	1.8M gates
Memory and ADC	18.4M bit / 4 ADC
Supply Voltage	1.2V core, 3.3V I/O
Active Power	310mW typical
Die Size	7.0mm x 7.0mm
Package	12mm x 12mm 144FBGA

Fig. 7 Die micrograph and Summary