

(1) ISEを使用して、  
VHDLシミュレーションをする。

# 必要ファイルを以下よりダウンロード

吉田先生の教科書サポートページ

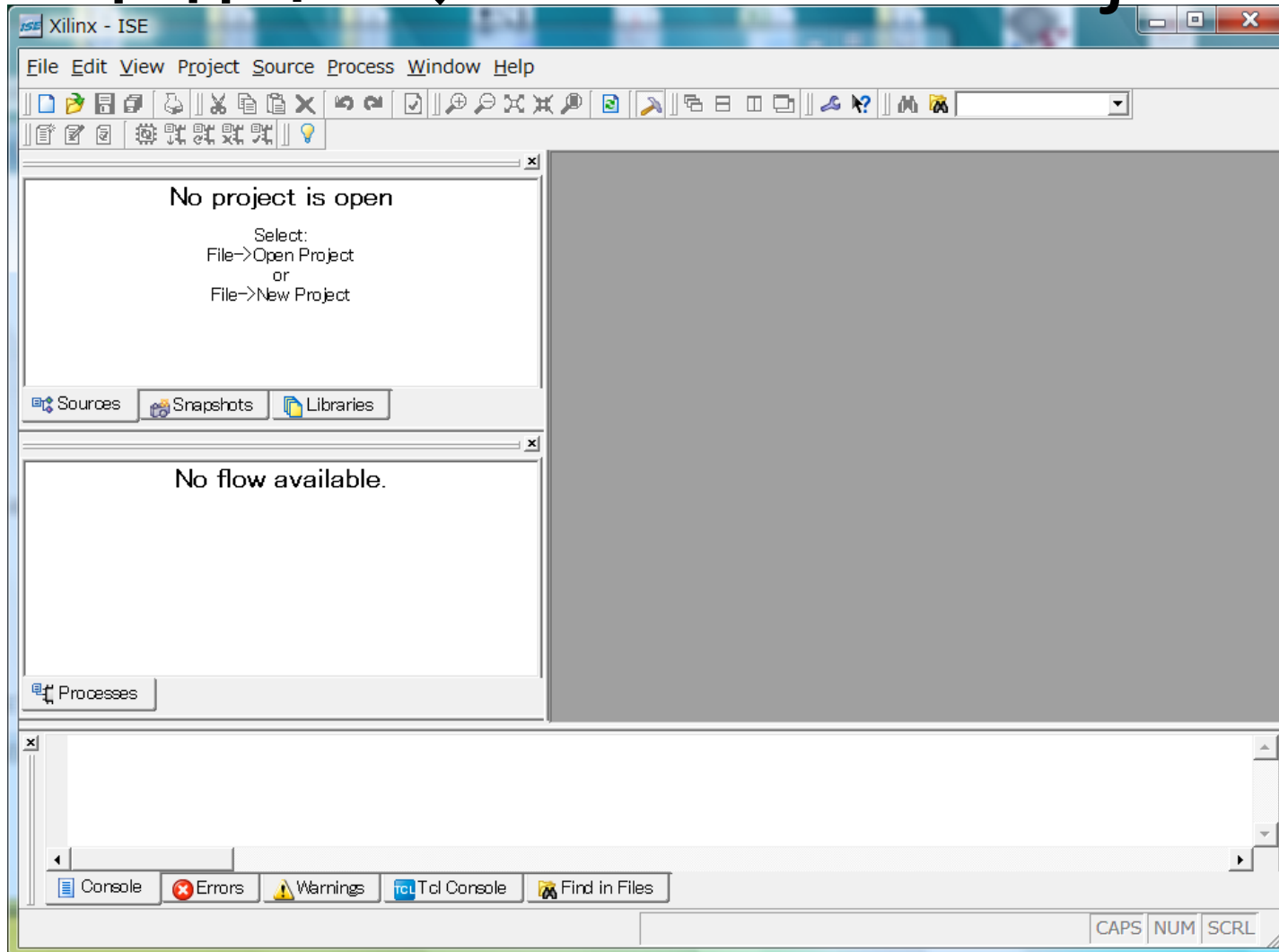
- [http://www.fts.ie.u-ryukyu.ac.jp/support/vhdl\\_digital/VHDL-src.html](http://www.fts.ie.u-ryukyu.ac.jp/support/vhdl_digital/VHDL-src.html)
- [3. HALF\\_ADDER-std.vhd](#)
- [14. TESTBENCH HA.vhd](#)



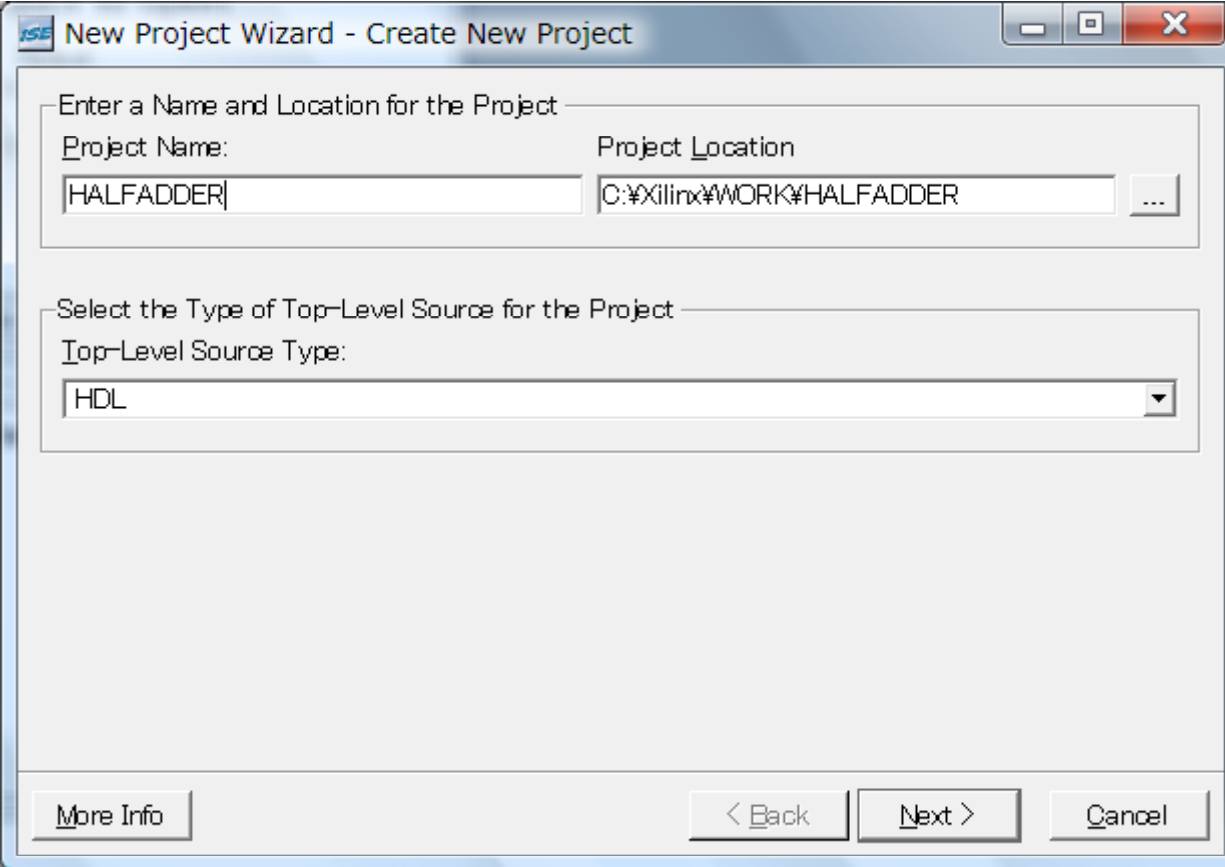
The screenshot shows a web browser window titled 'VHDLソースファイル一覧 - Windows Internet Explorer'. The address bar shows the URL 'fts.ie.u-ryukyu.ac.jp/support/vhdl\_digital/VHDL-src.html'. The page content is titled 'HDLソースファイル一覧' and includes a table with the following data:

No.	回路名	掲載ページ	リスト番号	VHDLファイル (Verilog-HDLファイル(*1))	論理合成(*2) シミュレーション(*3)
1	半加算器 (bit型使用)	24	2.1	<a href="#">HALF_ADDER-bit.vhd</a> ( <a href="#">HALF_ADDER.v</a> )	
2	全加算器のキャリー生成回路	47	3.1	<a href="#">FA_CARRY.vhd</a> ( <a href="#">FA_CARRY.v</a> )	
3	半加算器 (std_logic型使用)	59	4.1	<a href="#">HALF_ADDER-std.vhd</a> ( <a href="#">HALF_ADDER.v</a> )	
4	全加算器 (コンポーネント使用)	60	4.2	<a href="#">FULL_ADDER.vhd</a> ( <a href="#">FULL_ADDER.v</a> )	
5	4ビット加算器 (コンポーネント使用)	62	4.3	<a href="#">ADDER4-comp.vhd</a> ( <a href="#">ADDER4-comp.v</a> )	
6	4ビット加算器 (算術演算子使用)	63	4.4	<a href="#">ADDER4-op.vhd</a> ( <a href="#">ADDER4-op.v</a> )	
7	4ビットマルチプレクサ (セレクタ)	66	4.5	<a href="#">MULTIPLIER4.vhd</a> ( <a href="#">MULTIPLIER.v</a> )	
8	4ビットデマルチプレクサ	68	4.6	<a href="#">DEMULTIPLIER4.vhd</a> ( <a href="#">DEMULTIPLIER.v</a> )	

# ISEを起動して この画面で、File-> New Project



# お好みのディレクトリと プロジェクト名を設定



The image shows a screenshot of the "New Project Wizard - Create New Project" dialog box in the ISE software. The dialog box is titled "ISE New Project Wizard - Create New Project" and has standard Windows window controls (minimize, maximize, close) in the top right corner. The main content area is divided into two sections. The first section is titled "Enter a Name and Location for the Project" and contains two input fields: "Project Name:" with the text "HALFADDER" and "Project Location:" with the text "C:\Xilinx\WORK\HALFADDER". The "Project Location" field has a browse button ("...") to its right. The second section is titled "Select the Type of Top-Level Source for the Project" and contains a dropdown menu labeled "Top-Level Source Type:" with "HDL" selected. At the bottom of the dialog box, there are three buttons: "More Info", "< Back", and "Next >", and a "Cancel" button on the far right.

ISE New Project Wizard - Create New Project

Enter a Name and Location for the Project

Project Name: HALFADDER

Project Location: C:\Xilinx\WORK\HALFADDER

Select the Type of Top-Level Source for the Project

Top-Level Source Type: HDL

More Info < Back Next > Cancel

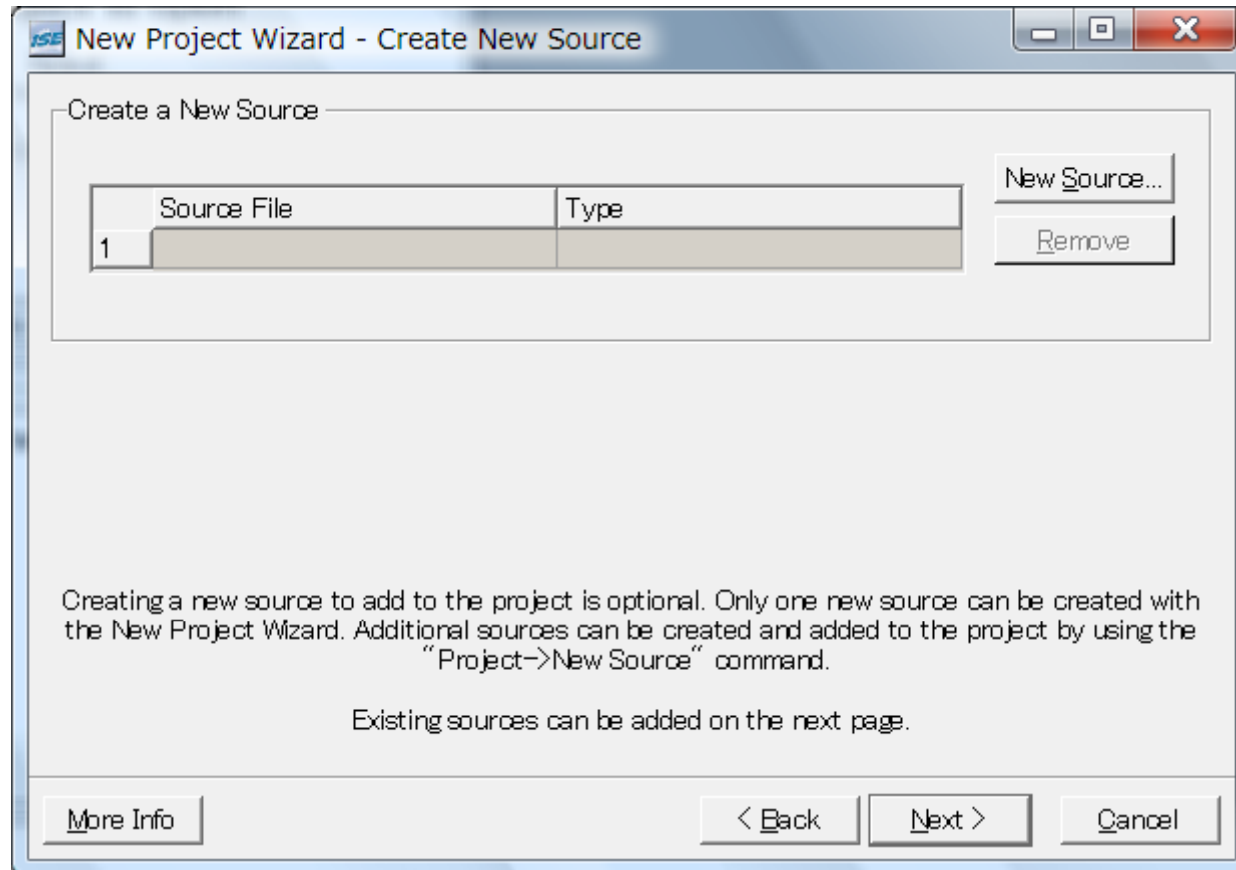
# ここは設定なし

Select the Device and Design Flow for the Project

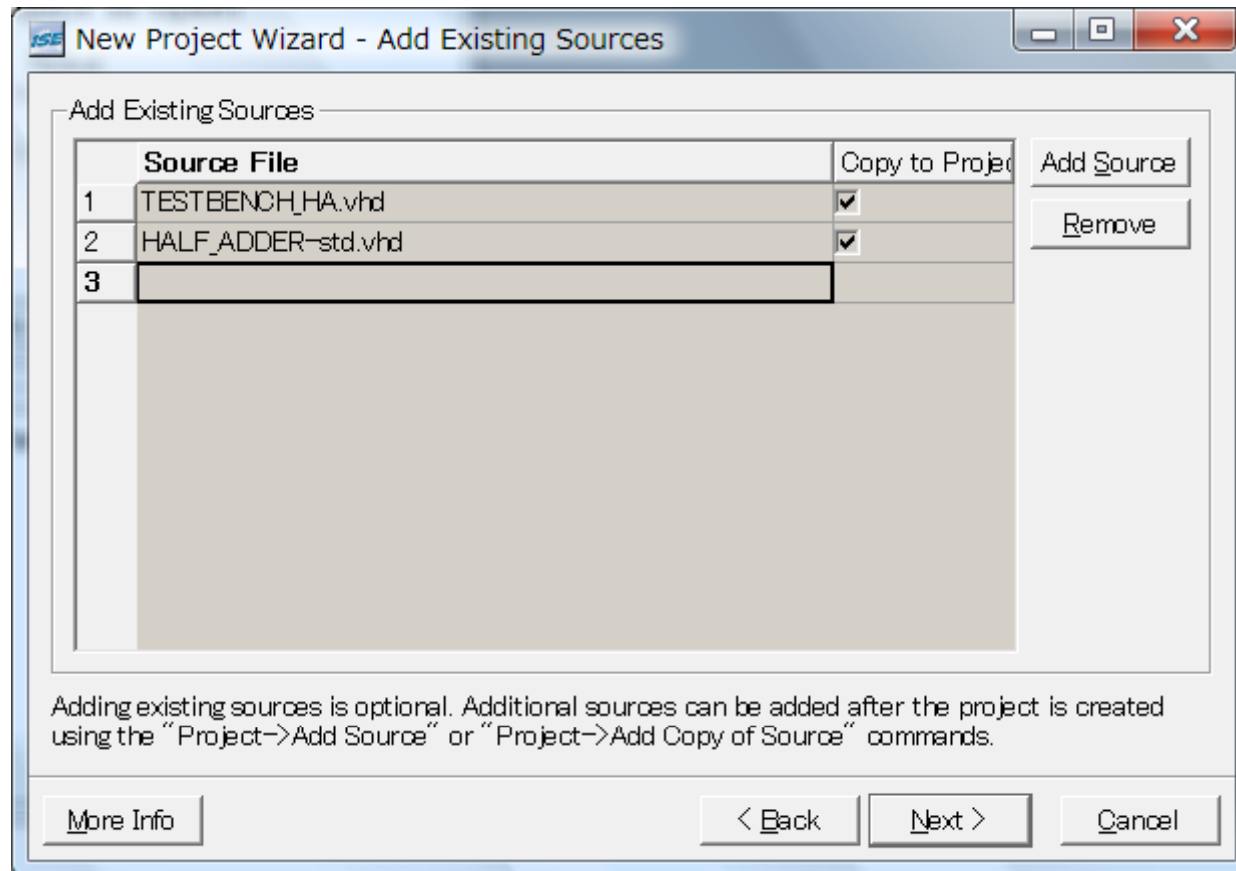
Property Name	Value
Product Category	All
Family	Automotive CoolRunner2
Device	Automatic xa2c000
Package	*
Speed	-*
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary	<input checked="" type="checkbox"/>
Enable Message Filtering	<input type="checkbox"/>
Display Incremental Messages	<input type="checkbox"/>

[More Info](#)      < [Back](#)      [Next >](#)      [Cancel](#)

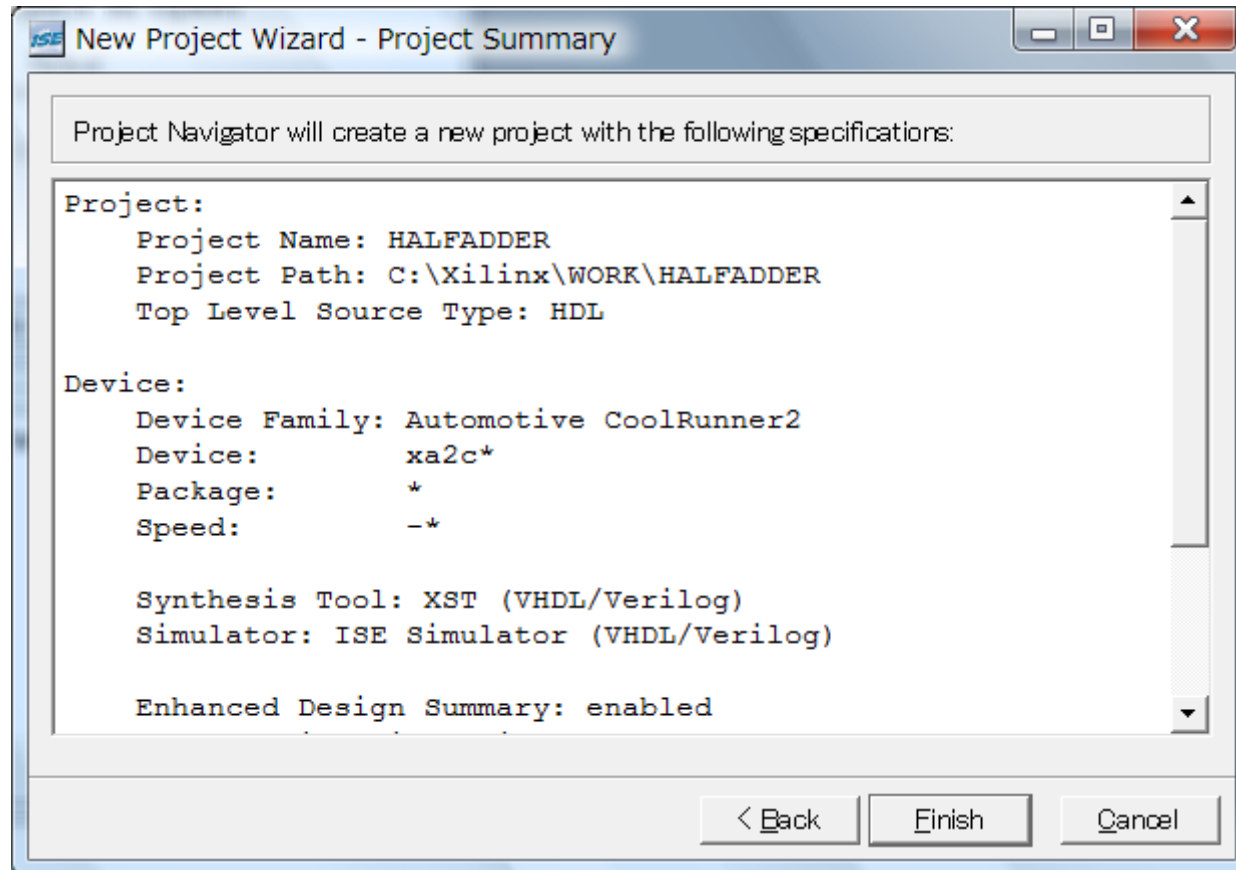
# ここも、設定なし



# Add\_Sourceで、 シミュレーションファイルを追加

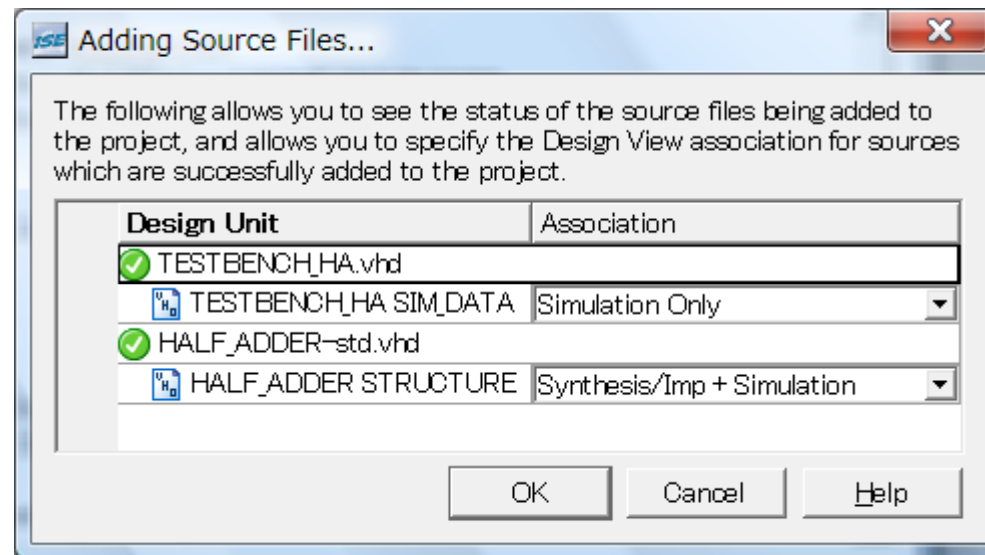


# 設定を確認し、Finish

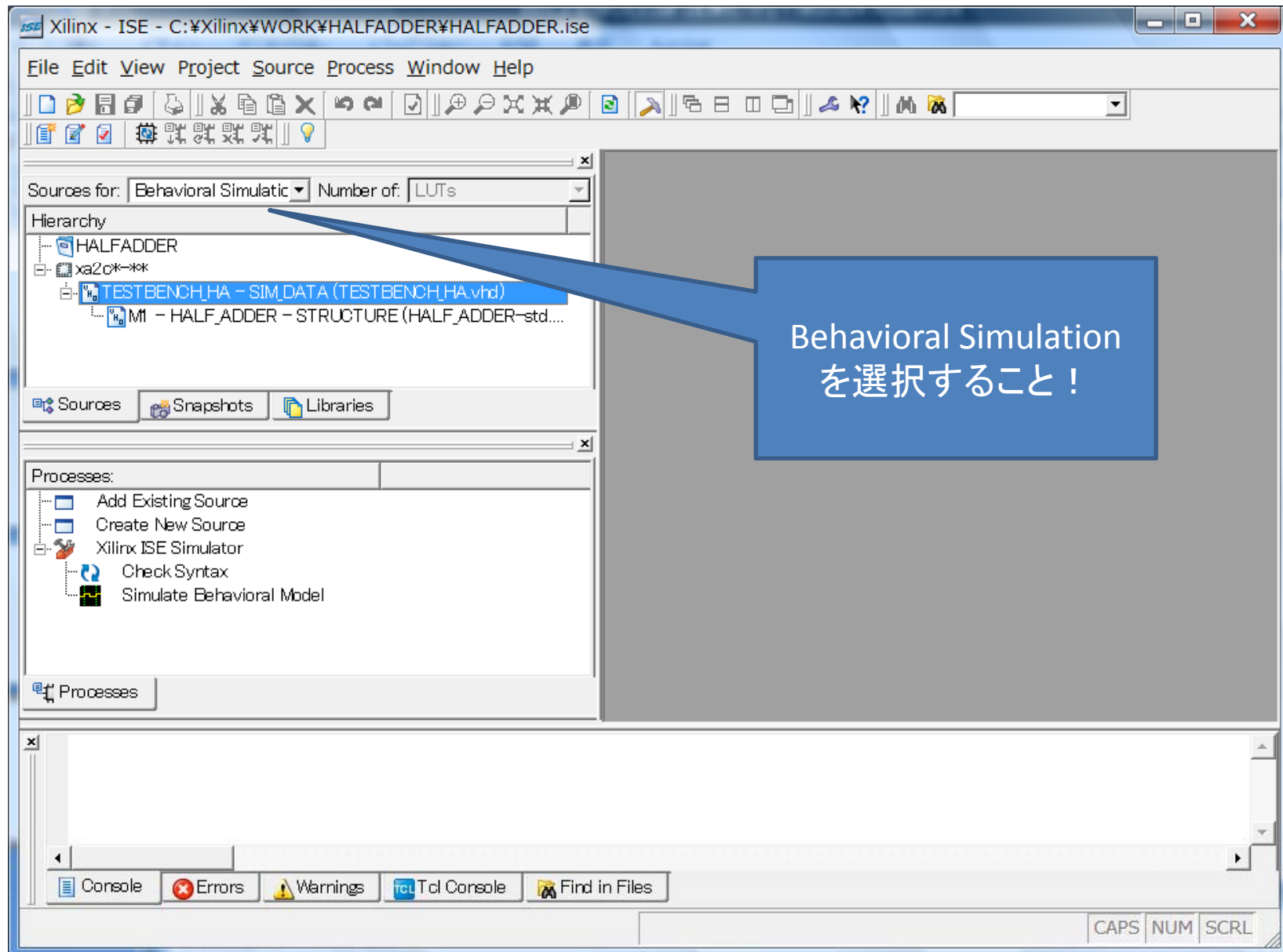




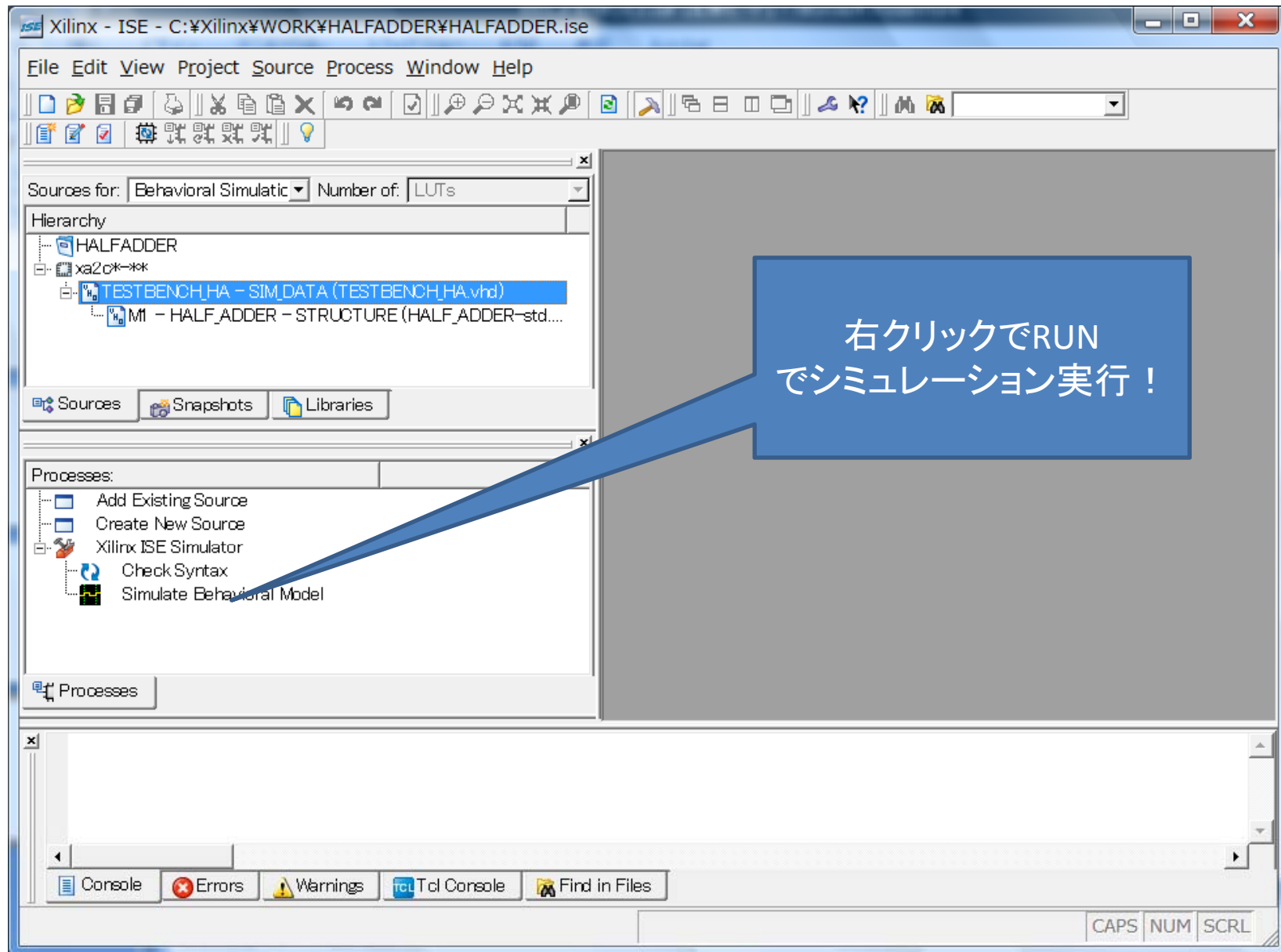
# 確認し、OK!



# このようになればOK！



# シミュレーション実行方法



# シミュレーション実行され、 動作波形が表示されます！

The screenshot shows the Xilinx ISE simulation environment. The main window displays a timing diagram for a half adder circuit. The diagram shows four signals: sa, sb, ss, and sc. The time axis ranges from 0 ns to 1000 ns. The signals are initialized to 0. The simulation is currently at 1000 ns. The console window at the bottom shows the following text:

```
This is a Full version of ISE Simulator:  
  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.
```

The console window also shows the following tabs: Console, Errors, Warnings, Tcl Console, Find in Files, and Sim Console - TESTBENCH\_HA. The status bar at the bottom right indicates the time: 462.0 ns.

# アナウンス

- 次回 10/19はツール関連の指導をTAより実施予定
  - TA: ファイヤー和田研M2 宮野智法
  - [tomo@lsi.ie.u-ryukyu.ac.jp](mailto:tomo@lsi.ie.u-ryukyu.ac.jp)
- 10/26はオンラインテスト(1回目)で、本日のデモに類することを各自のコンピュータで行っていただく予定です。