```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_SIGNED.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity MUL24 is
    Port ( XX  : in  STD_LOGIC_VECTOR (23 downto 0);
           YY  : in  STD_LOGIC_VECTOR (23 downto 0);
           ZZ  : out STD_LOGIC_VECTOR (23 downto 0);
                          ZZB : in  STD_LOGIC_VECTOR (23 downto 0);
                          XXB : out STD_LOGIC_VECTOR (23 downto 0);
                          YYB : out STD_LOGIC_VECTOR (23 downto 0));
end MUL24;

architecture Behavioral of MUL24 is

signal tmp, tmp1, tmp2 : std_logic_vector(47 downto 0);

begin

tmp <=  XX  * YY;
ZZ  <= tmp(39 downto 16);

tmp1 <= ZZB * YY;
XXB  <= tmp1(39 downto 16);

tmp2 <= ZZB * XX;
YYB  <= tmp2(39 downto 16);

end Behavioral;
```