```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_SIGNED.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity RELU_FUNC is
    Port ( XX  : in  STD_LOGIC_VECTOR (23 downto 0);
           YY  : out STD_LOGIC_VECTOR (23 downto 0);
                          YYB : in  STD_LOGIC_VECTOR (23 downto 0);
                          XXB : out STD_LOGIC_VECTOR (23 downto 0));
end RELU_FUNC;



architecture Behavioral of RELU_FUNC is

begin

process(XX) begin
  if (XX(23) = '1') then
    YY <= "000000000000000000000000";
  else
    YY <= XX;
  end if;
end process;

process(YYB, XX) begin
  if (XX(23) = '1') then
    XXB <= "000000000000000000000000";
  else
    XXB <= YYB;
  end if;
end process;

end Behavioral;
```