```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY TEST_NN IS
END TEST_NN;

ARCHITECTURE behavior OF TEST_NN IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT NN2019_BP
    PORT(
         RESET  : in  STD_LOGIC;
         SYSCLK : in  STD_LOGIC;
         COUNT2 : out STD_LOGIC_VECTOR ( 1 downto 0);
         A41    : out STD_LOGIC_VECTOR (23 downto 0);
         A42    : out STD_LOGIC_VECTOR (23 downto 0)
        );
    END COMPONENT;

   --Inputs
   signal RESET  : std_logic := '0';
   signal SYSCLK : std_logic := '0';

         --Outputs
   signal COUNT2 : std_logic_vector (1 downto 0);
   signal A41    : std_logic_vector (23 downto 0);
   signal A42    : std_logic_vector (23 downto 0);

   -- Clock period definitions
   constant SYSCLK_period : time := 10 ns;

BEGIN

         -- Instantiate the Unit Under Test (UUT)
   uut: NN2019_BP PORT MAP (
         RESET => RESET,
         SYSCLK => SYSCLK,
                         COUNT2 => COUNT2,
```

```
                        A41 => A41,
                        A42 => A42
        );

   -- Clock process definitions
   SYSCLK_process :process
   begin
                SYSCLK <= '0';
                wait for SYSCLK_period/2;
                SYSCLK <= '1';
                wait for SYSCLK_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;
      RESET <= '1';

      wait;
   end process;

END;
```