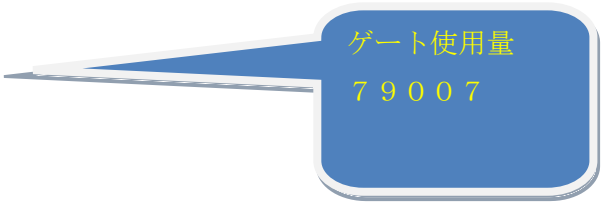
```
=========================================================================
*                          Final Report                                 *
=========================================================================
Final Results
RTL Top Level Output File Name     : NN2019_BP.ngr
Top Level Output File Name         : NN2019_BP
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 52

Cell Usage :
# BELS                             : 79007
#      BUF                         : 2
#      GND                         : 1
#      INV                         : 210
#      LUT1                        : 555
#      LUT2                        : 11991
#      LUT2_D                      : 1
#      LUT2_L                      : 2
#      LUT3                        : 2096
#      LUT3_D                      : 2
#      LUT3_L                      : 2
#      LUT4                        : 9452
#      LUT4_D                      : 5
#      MULT_AND                    : 8637
#      MUXCY                       : 23149
#      VCC                         : 1
#      XORCY                       : 22901
# FlipFlops/Latches                : 717
#      FDC                         : 516
#      FDP                         : 201
# Clock Buffers                    : 1
#      BUFGP                       : 1
```



IO Buffers : 51
IBUF : 1
OBUF : 50
DSPs : 32
DSP48 : 32

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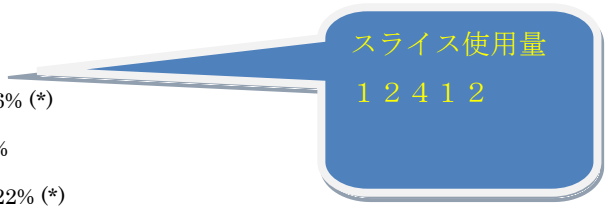
Device utilization summary:

Selected Device : 4vfx12ff668-10

Number of Slices:	12412	out of 5472	226% (*)
Number of Slice Flip Flops:	717	out of 10944	6%
Number of 4 input LUTs:	24316	out of 10944	222% (*)
Number of IOs:	52		
Number of bonded IOBs:	52	out of 320	16%
Number of GCLKs:	1	out of 32	3%
Number of DSP48s:	32	out of 32	100%



WARNING:Xst:1336 - (*) More than 100% of Device resources are used

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Partition Resource Summary:

No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

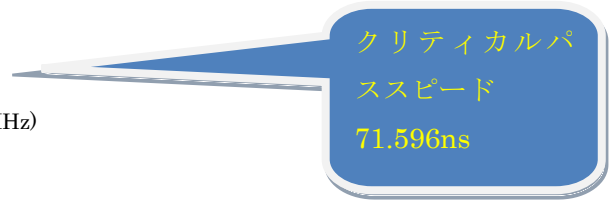
Clock Signal	Clock buffer(FF name)	Load
SYSCLK	BUFGP	717

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
RESET_inv(RESET_inv301_INV_0:O)	NONE(B21_0)	359
RESET_inv301_INV_0_1(RESET_inv301_INV_0_1:O)	NONE(W311_10)	358

Timing Summary:

Speed Grade: -10



Minimum period: 71.596ns (Maximum Frequency: 13.967MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 44.460ns

Maximum combinational path delay: No path found